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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HESSELTINE, RYAN J	
ART UNIT	**PAPER NUMBER**
2623	

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/458,370	Applicant(s) LIPPINCOTT, LOUIS A.	
	Examiner Ryan J Hesseltine	Art Unit 2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8,11-15,19-21,23-25 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8,11-15,19-21,23-25 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 12, filed January 21, 2004, with respect to claims 1, 15, and 23 have been fully considered and are persuasive. The objection of claims 1, 15, and 23 has been withdrawn.

2. The rejection of claims 2, 3, 9, 10, 16, 17, and 26 are rendered moot by applicant's cancellation of those claims.

3. Applicant's arguments on pages 9-11, filed January 21, 2004 with respect to Tanaka et al. have been fully considered but they are not persuasive. Page 9, second paragraph states, "the interpretation of the Tanaka references mixes the different Tanaka embodiments." The examiner understands that different sections of the Tanaka reference are cited and that some of those sections come from different embodiments, but the examiner is not attempting to mix these embodiments to teach or suggest the instant invention. For clarity, the examiner has removed many references relying on other embodiments disclosed by Tanaka. The examiner believes that teachings from different embodiments are not needed to anticipate applicant's invention.

4. Page 10, bottom of first paragraph states, "The address at which the data is read out is admittedly changed, but nowhere is there any teaching or suggestion that both of the calculators are calculating data in the same direction at the same time." The examiner respectfully disagrees. Tanaka discloses that initially, addresses are designated in a row direction such that the calculated results from the one-dimensional DCT calculator 4 are written to the memory device 2 in a row direction (column 11, line 9-15). Next, the address direction is switched to designate addresses in a column direction wherein addresses are read from the memory device 2

in a column direction. Once the first memory location (0,0) is **read and transmitted** to the one-dimensional DCT calculator 6, the calculated results of the one-dimensional DCT calculator 4 are **written to the same address** (0,0) as data. Then the memory address is changed to (0,1) (incremented in the column direction) and the one-dimensional DCT calculator 6 **reads data of this address**. Subsequently, the calculated results of the one-dimensional DCT calculator 4 are **written to this address** (0,1) as data and such reading and writing operations are repeatedly performed until the last memory address (column 11, line 16-34; see also column 10, line 64-column 11, line 5). Tanaka then discloses that the **row and column addresses** in the memory device are **switched** again at which time the one-dimensional DCT calculator 6 **reads data out** of a memory address in a **row direction** and the calculated results of the one-dimensional DCT calculator 4 are then **written to the same address** until the last address (column 11, line 34-40; see also column 10, line 26-31 and 59-63). This explicit explanation of the first embodiment shown in Tanaka's Figures 5-10 clearly shows all of the claimed limitations.

Claim Objections

5. Claim 19 is objected to because of the following informalities: line 7 was amended to recite, "execute a third one dimensional inverse discrete..." Line 10 was also amended in a similar way. The examiner believes that applicant did not intend to change line 7 from "second" to "third" in accordance with the reference made to a "second function" on line 11 of claim 19, and in accordance with similar claim 15. Appropriate correction is required.

6. Claim 23 is objected to because of the following informalities: line 7 was amended to state, "a first to state to" (emphasis added). The examiner believes applicant intended this to read "a first state to..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 15 and 19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 15 and 19 recite limitations pertaining to executing a first one-dimensional (1-D) inverse discrete cosine transforming (IDCT) function on a first inverse discrete cosine calculator in a row direction on a first matrix of coefficients to produce a first matrix of intermediate results. Later in the claims, a third 1-D IDCT function is performed on said first inverse discrete cosine calculator in a column direction on the first matrix of intermediate results. This is in direct contradiction with the specification and drawings. Also, after said first executing, on a second inverse discrete cosine calculator, a second 1-D IDCT is executed in a column direction on a second matrix of coefficients to produce another matrix of intermediate results. This matrix of intermediate results is not again mentioned in the claims. It is believed that applicant intended to claim that the first inverse discrete cosine calculator operates on a first matrix of coefficients in a row direction to produce a first matrix of intermediate results. Subsequently, the same first inverse discrete cosine calculator operates in a second matrix of coefficients in a column direction to produce another matrix of intermediate results. Concurrently, a second inverse discrete cosine

calculator operates on the first matrix of intermediate results in a column direction. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 4-8, 11-15, 19-21, 23-25 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (USPN 5,268,853, previously cited), hereafter Tanaka.

11. Regarding claim 1, Tanaka discloses a method of implementing a two-dimensional inverse discrete cosine transform (column 4, line 61-68; column 13, line 23-25), comprising: executing first and second one-dimensional inverse discrete cosine transforming functions in first and second separate inverse discrete cosine transforming calculators (4, 6), each of the first and second functions being controlled to operate on a matrix of coefficients (Figure 5; column 5, line 12-33) with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in a row direction at a first time (column 11, line 9-15), and with both of said fist and second inverse discrete cosine transforming calculators operating simultaneously in a column direction at a second time (column 11, line 16-40; column 15, line 10-28).

12. Regarding claim 8, Tanka discloses a storage medium bearing a machine-readable program capable of causing a machine to: execute two, one-dimensional inverse discrete cosine transforming functions (column 4, line 61-68; column 13, line 23-25) in first and second inverse discrete cosine calculators (4, 6), each of the functions being controlled to operate on a matrix of

coefficients (Figure 5; column 5, line 12-33) with both of said first and second inverse discrete cosine transforming calculators operating simultaneously in the row direction at a first time (column 11, line 9-15), and with both of said fist and second inverse discrete cosine transforming calculators operating simultaneously in the column direction at a second time subsequent to said first time (column 11, line 16-40; column 15, line 10-28).

13. Regarding claim 15, Tanaka discloses a method of implementing a two-dimensional inverse discrete cosine transform (column 4, line 61-68; column 5, line 12-33; column 13, line 23-25), comprising: first executing a first one-dimensional inverse discrete cosine transforming function on a first inverse discrete cosine calculator (4), in a row direction on a first matrix of coefficients to produce a first matrix of intermediate results (Figure 5; column 11, line 9-15); second, after said first executing, on a second inverse discrete cosine calculator (6), executing a second one-dimensional inverse discrete cosine transform in a column direction on a second matrix of coefficients to produce another matrix of intermediate results; on said first inverse discrete cosine calculator (4), executing a third one-dimensional inverse discrete cosine transforming function in said column direction on the first matrix of intermediate results concurrent with said second executing in the column direction on said second matrix of coefficients (column 11, line 18-40), and periodically switching and executing between the row and column directions (column 10, line 26-31 and 59-63; column 11, line 16-17; column 15, line 10-28).

14. Regarding claim 19, Tanaka discloses a storage medium bearing a machine-readable program capable of causing a machine to: execute a first one-dimensional inverse discrete cosine transforming function (Figure 5, element 4), where the first function executes in a row direction

on a first matrix of coefficients, producing a matrix of intermediate results (column 11, line 9-15); execute a third one-dimensional inverse discrete cosine transform (Figure 5, element 4) in a column direction on a second matrix of coefficients; execute a third one-dimensional inverse discrete cosine transforming function (Figure 5, element 6), where the second function executes in said column direction on the matrix of intermediate results concurrent with execute a second function on the second matrix of coefficients (column 11, line 18-40), in which the functions switch periodically and concurrently between the row and column directions (column 10, line 26-31 and 59-63; column 11, line 16-17; column 15, line 10-28).

15. Regarding claims 23 and 25, Tanaka discloses an apparatus/computer implementing a two-dimensional inverse discrete cosine transform (column 4, line 61-68; column 5, line 12-33; column 13, line 23-25), comprising: two (first and second) one-dimensional inverse discrete cosine transform blocks (Figure 5, elements 4 and 6); a memory block (Figure 5, element 2); a sequencer block (Figure 6, element 18), the sequencer block alternately being in a first state to control a column direction of operation of both one-dimensional inverse discrete cosine transform, and in a second state to control a row direction of operation of both one-dimensional inverse discrete cosine transform blocks (column 10, line 17-31; column 11, line 9-20); and an address generator block (Figure 5, element 8) which generates addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer (column 6, line 35-42 and 56-65; column 9, line 59-68).

16. Regarding claims 4 and 11, Tanaka discloses that a sequencer determines which direction each function operates in for a given matrix (figure 6, element 18; column 11, line 16-17).

17. Regarding claims 5 and 12, Tanaka discloses that an address generator which generates an address for each coefficient in the matrix (column 5, line 55-59).

18. Regarding claims 6 and 13, Tanaka discloses that the functions concurrently executed in the same direction on two different matrices of coefficients (column 11, line 16-40; column 12, line 4-10).

19. Regarding claims 7 and 14, Tanaka discloses that the functions are concurrently executed in the same direction (column 12, line 4-10), the functions switching periodically and concurrently to the other direction (column 11, line 16-40; column 15, line 10-28).

20. Regarding claim 28, Tanaka discloses that said second one-dimensional inverse discrete cosine transforming function and said third one-dimensional inverse discrete cosine transforming function occur concurrently in the same direction (column 11, line 16-40; column 15, line 10-28).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USPN 4,760,543 to Ligtenberg et al. discloses an orthogonal transform processor. USPN 4,791,598 to Liou et al. discloses a two-dimensional discrete cosine transform processor. USPN 4,829,465 to Knauer et al. discloses a high-speed cosine transform. USPN 5,181,183 to Miyazaki discloses a discrete cosine transform circuit suitable for integrated circuit implementation. USPN 5,412,740 to Fadavi-Ardekani discloses a signal processing system having reduced memory space.

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J Hesseltine whose telephone number is 703-306-4069. The examiner can normally be reached on Monday - Friday, 8:30 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on 703-308-6604. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

rjh
March 25, 2004

JINGGE WU
PRIMARY EXAMINER